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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,101	03/13/2007	Sacha Romier	DE03 0228 US1	8087

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EXAMINER	
HUYNH, PHUONG	

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
08/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/562,101	ROMIER ET AL.	
	Examiner	Art Unit	
	PHUONG HUYNH	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/01/2008 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Holloway et al. (hereinafter "Holloway") (US Patent No. 6,183,131).

Regarding claim 1, Holloway discloses an arrangement on a semiconductor chip for calibrating a temperature setting curve having

a signal generation unit for providing a first signal which is proportional to the actual temperature of the chip, whereby a signal offset creatable by the signal generation unit, which is combined with the first signal to define a second signal [see Holloway: col. 11, lines 15-50];

a temperature extraction unit [A/D and summing circuits 114] receiving the first signal and the second signal calculating a first temperature point based on the first signal and for calculating a second temperature point based on the second signal, wherein the second temperature point is a virtual temperature point and wherein the first and second temperature points are different from each other [computed/calculated Tout(K), or Tout(C)] [see Holloway: col. 7, lines 7-67, lines col. 11, line 40-col. 12, line 6].

Regarding claim 2, Holloway discloses that the first signal which is proportional to the actual temperature of the chip, is a current, voltage or a frequency [see Holloway: col. 11, lines 15-40].

Regarding claim 3, Holloway discloses that the first signal and the second signal are convertible into digital signals, whereby the extraction unit calculates the first and second temperature points for calibrating the temperatures setting curves [see Holloway: col. 11, line 40-col. 12, line 6].

Regarding claim 4, Holloway discloses a method for calibrating a temperature setting curve of a temperature sensor arrangement on a semiconductor chip, the method comprising:

reading a first signal which is proportional to an actual temperature of the semiconductor chip [see Holloway: col. 11, lines 15-40]; generating a signal offset, which is combined with the first signal to define a second signal [see Holloway: col. 11, lines 40-47]; extracting a first temperature from the first signal and a second virtual temperature from the second signal; wherein the first and second virtual temperature are different from each other [see Holloway: col. 7, lines 7-67; col. 11, line 45-col. 12, line 25]; and
calibrating a temperature setting curve of the semiconductor chip using the first actual temperature and the second virtual temperature [see Holloway: col. 2, lines 6-20; col. 11, line 40-col. 12, line 25].

Regarding claim 5, Holloway discloses whereby the first actual temperature and the second virtual temperature are used for providing calibration parameters to the semiconductor chip [see Holloway: col. 7, lines 7-67; col. 11, line 45-col. 12, line 6].

Regarding claim 6, Holloway discloses whereby calculating calibration parameters can be performed on-chip *or* off-chip [see Holloway: Abstract; col. 7, lines 7-67; col. 11, line 45-col. 12, line 6].

Regarding claim 7, Holloway discloses whereby additional offsets are provided for calculating more than two temperature points and calibrating the temperature setting curve [see Holloway: col. 2, lines 6-20; col. 11, line 40-col. 12, line 25].

Regarding claim 8, Holloway discloses that whereby the signal offset is subtracted from the first signal or added to the first signal defining a second signal, which is provided to the temperature extraction unit [see Holloway: col. 11, line 45-col. 12, line 25].

Regarding claims 9 and 10, Holloway discloses that the second temperature point [computed Tout(K) or Tout(C)] does not exist in the semiconductor chip during calibration of the temperature setting curve [see Holloway: col. 11, lines 5-50].

Response to Arguments

3. Applicants' arguments filed 08/01/2008 have been fully considered but they are not persuasive.

Applicants argue that "In contrast to Holloway, amended claim 1 recites that two temperature points (the first and second temperature points) are calculated from a single dependent signal (the first signal) ...and that Holloway does not disclose one of the temperature points is a virtual temperature and Holloway does not anticipate the amended claim 1" [see Applicants' Remarks: Page 5].

Accordingly, amended claim 1 recites "a temperature extraction unit [A/D and summing circuits 114] receiving the first signal and the second signal calculating a first temperature point based on the first signal and for calculating a second temperature point based on the second signal [see amended claim 1, lines 7-9]"; not "two temperature points (the first and second temperature points) are calculated from a single dependent signal (the first signal)".

Further, Holloway discloses "wherein the second temperature point is a virtual temperature point" as recited in amended claim 1 [see Holloway: col. 7, lines 7-67, lines col. 11, line 40-col. 12, line 6; or see the above rejection in this Office Action].

Accordingly, Holloway discloses the claimed invention as recited in amended claim 1 [see the above rejection in this Office Action].

Regarding amended claim 4, Applicants argue that "in view of similarities between amended claims 1 and 4, Applicants assert that the remarks provided in regard to amended claim 1 apply also to amended claim 4. Accordingly, Applicants assert that amended claim 4 is not anticipated by Holloway" or "Holloway does not disclose "using two different temperatures, which were generated from the temperature-dependent signal, to calibrate a temperature setting curve" as recited in amended claim 4" [see Applicants' Remarks: Page 6].

Accordingly, Holloway discloses the claimed invention as recited in amended claim 4 [see the rejection of claim 4 above in this Office Action].

Further, amended claim 4 recites "calibrating a temperature setting curve of the semiconductor chip using the first actual temperature and the second virtual temperature point" [see amended claim 4, lines 10-11]; not "using two different temperatures, which were generated from the temperature-dependent signal, to calibrate a temperature setting curve".

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUONG HUYNH whose telephone number is (571)272-2718. The examiner can normally be reached on M-F: 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Huynh
Examiner
Art Unit 2857

/Phuong Huynh/
Examiner, Art Unit 2857
August 11, 2008

/Eliseo Ramos-Feliciano/
Supervisory Patent Examiner, Art Unit 2857